the global wiring layer comprises:

a first wiring layer formed on the semiconductor substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer, and

inner bumps formed on the second wiring layer.--

Cancel claims 3-5.

Amend claim 6 as follows:

8. --~~6.~~ (amended) A system semiconductor device, comprising:

a system LSI cell portion which includes a plurality of functional blocks for realizing specific functions, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip; and

a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other, wherein:

the global wiring layer comprises;

a first wiring layer formed on an organic substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer, and

inner bumps formed on the second wiring layer.--

Amend claim 7 as follows:

3. ~~7.~~ (amended) A system semiconductor device as claimed in claim 1, wherein the insulating layer includes a via which electrically connects the first wiring layer with the second wiring layer.--

Cancel claim 8.

Amend claim 11 as follows:

6. ~~11.~~ (amended) A system semiconductor device as claimed in claim 1, wherein the global wiring layer has at least one or more of the insulating layers.--

Amend claim 12 as follows:

9. ~~12.~~ (amended) A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a plurality of functional blocks which are constructed to serve as unit circuits and realize specific functions on a semiconductor chip,

fabricating a global wiring layer separate from the fabricated system LSI cell portion by forming a wiring layer on a semiconductor substrate, and

laminating the system LSI cell portion with the separately fabricated global wiring layer such that the

functional blocks are electrically connected to each other.--

Amend claim 16 as follows:

18. --~~16~~. (amended) A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a plurality of functional blocks which serve as unit circuits and realize specific functions on a semiconductor chip,

fabricating a global wiring layer by forming a wiring layer on a semiconductor substrate, and

laminating the system LSI cell portion with the global wiring layer such that the functional blocks are electrically connected to each other;

wherein the global wiring layer is formed by sequentially laminating a first wiring layer, a second wiring layer, an insulating layer, and inner bumps on the semiconductor substrate.--

Amend claim 17 as follows:

19. --~~17~~. (amended) A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a plurality of functional blocks which serve as unit circuits and realize specific functions on a semiconductor chip,

fabricating a global wiring layer by forming a wiring layer on a semiconductor substrate, and

laminating the system LSI cell portion with the global wiring layer such that the functional blocks are electrically connected to each other;

wherein the global wiring layer is formed by sequentially laminating a first wiring layer, an insulating layer, a second wiring layer, and inner bumps on an organic substrate.--

Add the following new claim:

--~~23~~. (new) A system semiconductor device as claimed in claim 1, wherein the global wiring layer includes buried vias which electrically connect the functional blocks to an external circuit.--

Please charge the fee of $168 for the two extra independent claims added herewith, to Deposit Account No. 25-0120.

REMARKS

This application has been amended so as to place it in condition for allowance at the time of the next Official Action.

The Official Action rejects claims 1 and 12 under 35 USC §102(b) as being anticipated by YAMAZAKI et al. 5,300,798. Reconsideration and withdrawal of this rejection are respectfully requested for the following reasons:

The rejected claims constitute the two independent claims in the present application, reciting a device and a method of fabricating such device, respectively. Of the rejected